STM8 Core & Architecture

STM8 Technical Training

CONTENTS

Introduction

- The goal is to present you the new 8-bit core made in ST which will replace the ST7
- We will focus on the improvements of the STM8 versus the ST7

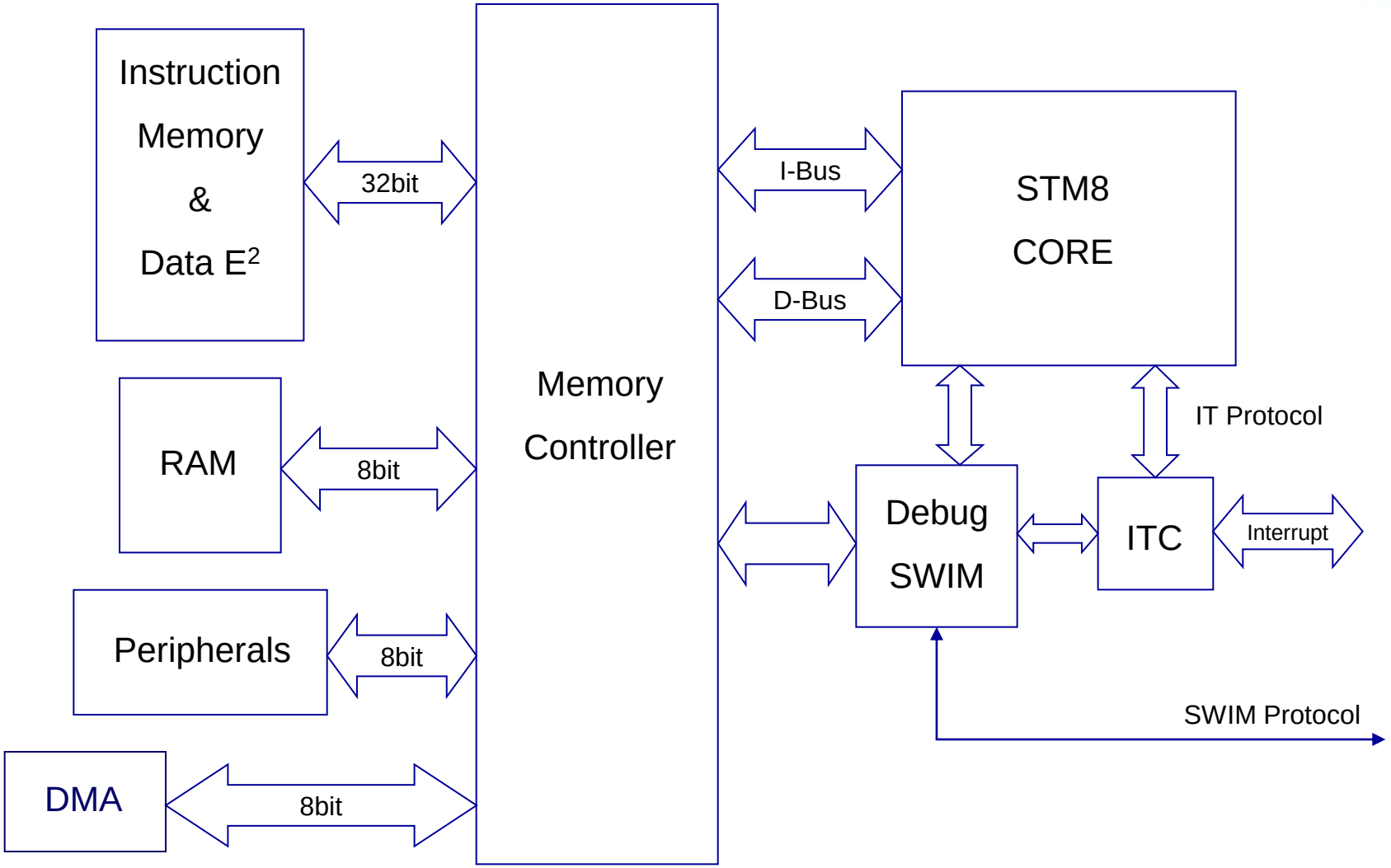
Architecture (1/2)

- **Harvard architecture**
  - 3-stage pipeline
  - CISC machine
  - Unified memory space
  - 32-bit program memory (EE/Flash) access
    - Pre-code only affects code density, not performance
  - 8-bit data access
    - Fast access to variables
    - Tightly connected RAM (register file extension)
  - Reduced CPI >> reduced clock frequency
    - Most of instructions executed in one cycle per instruction
  - Signed arithmetic operation support
  - Higher power efficiency

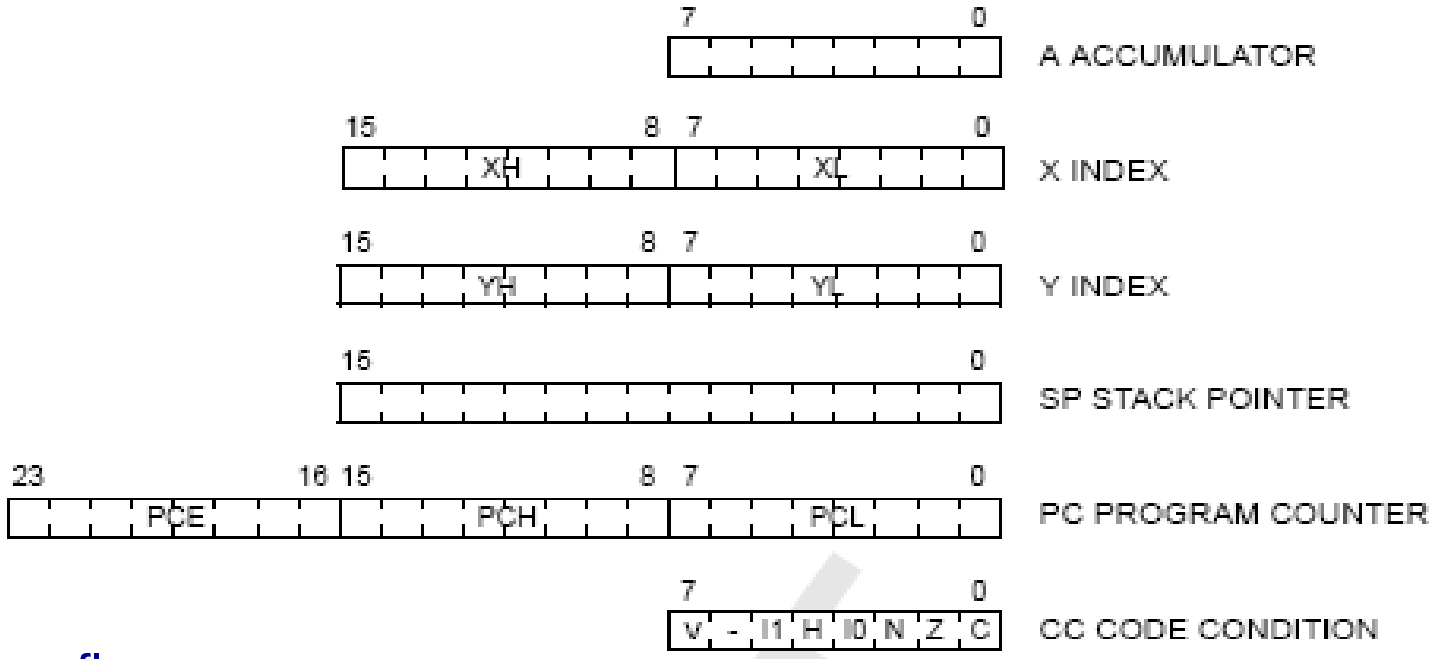
Architecture (2/2)

- **16Mbytes addressing space**
  - With a 24-bit Program Counter
- **16-bit index registers**
  - Remove all the limitations related to 0-page (1st 256 bytes of RAM)
    - Fast and bit accesses to whole RAM and register space
  - All indexed addressing modes will take advantage of full access to the 1st 64k segment access
  - Whole 0-page space available for global variables & literal pool
  - Benefits for Compiler in combination with new instruction set
    - More compact code for addressing tables in the whole 64k segment (8-bit offset only)
      - (off.b, X) addressing mode becomes much more powerful
    - Allows the usage of large arrays (>256 elements)
    - More efficient parameter passing onto the stack (using either SP or X/Y as frame pointer)
      - Standard memory model
      - Reentrance possible

STM8 System Implementation

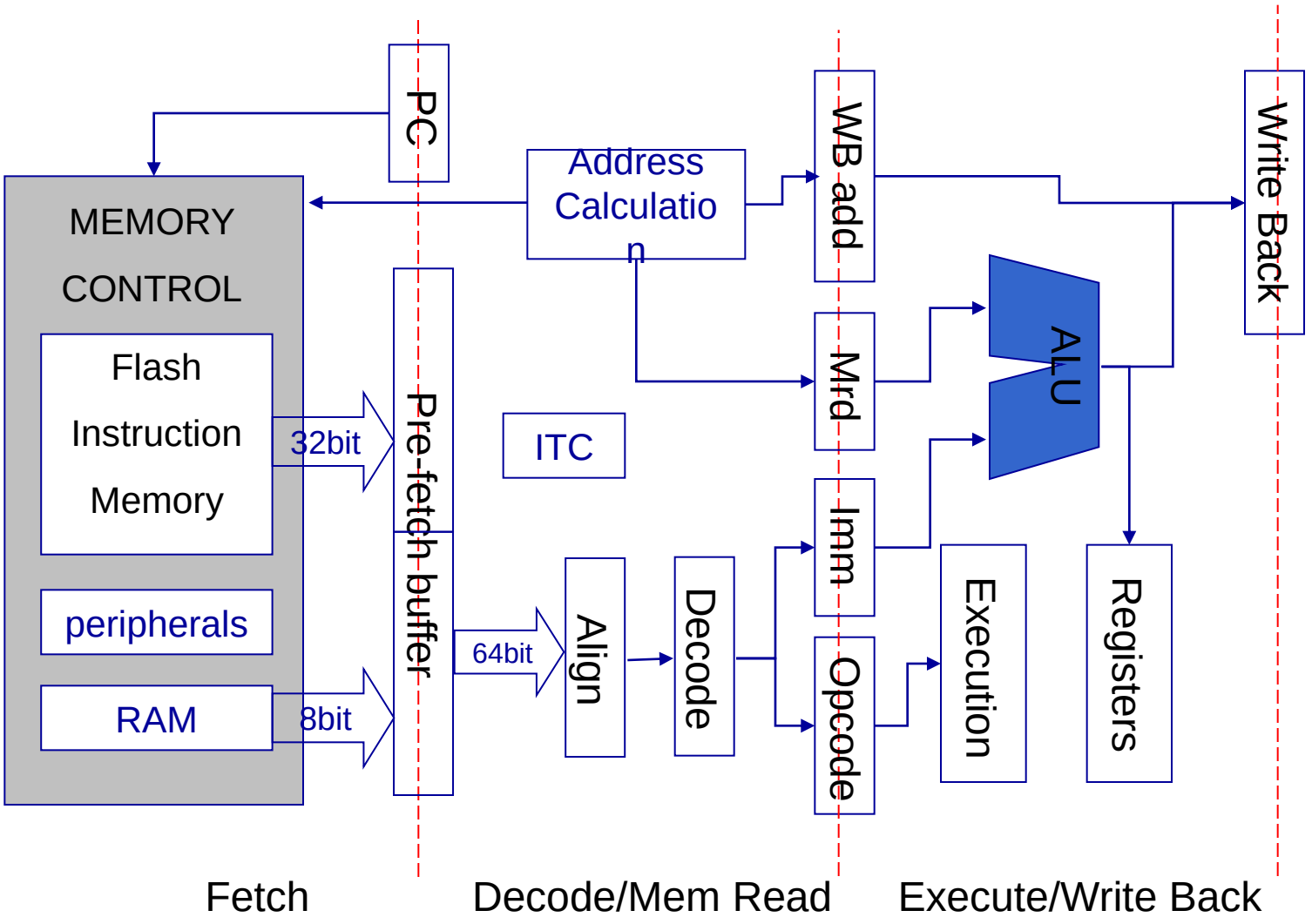


STM8 Core Register Set



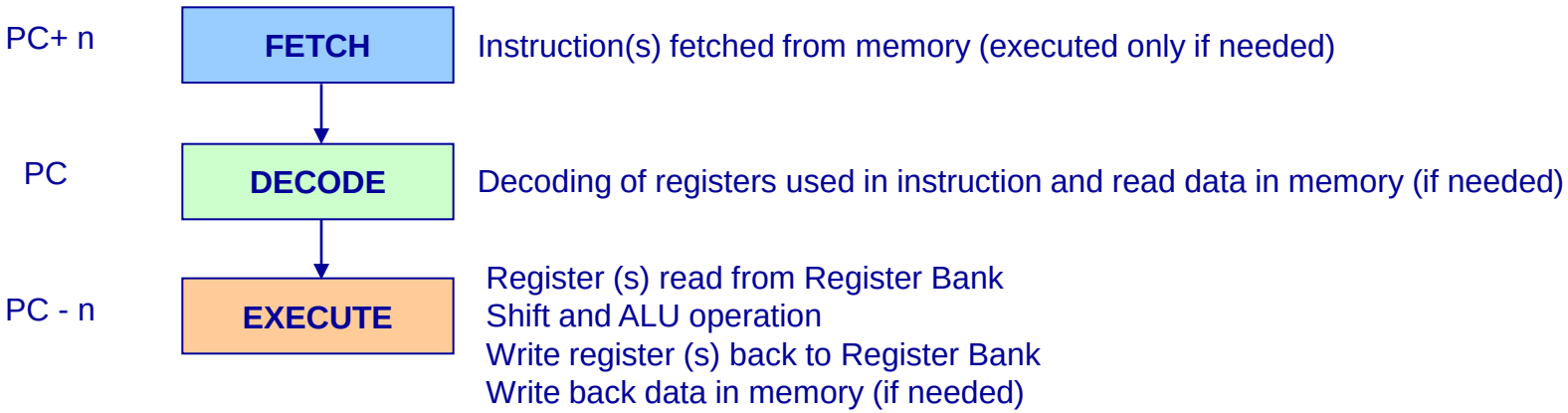
V: Overflow
H: Half-carry
N: Negative
Z: Zero
C: Carry
IO, I1: interrupt mask level 0, 1

CPU basic pipeline



The Instruction Pipeline

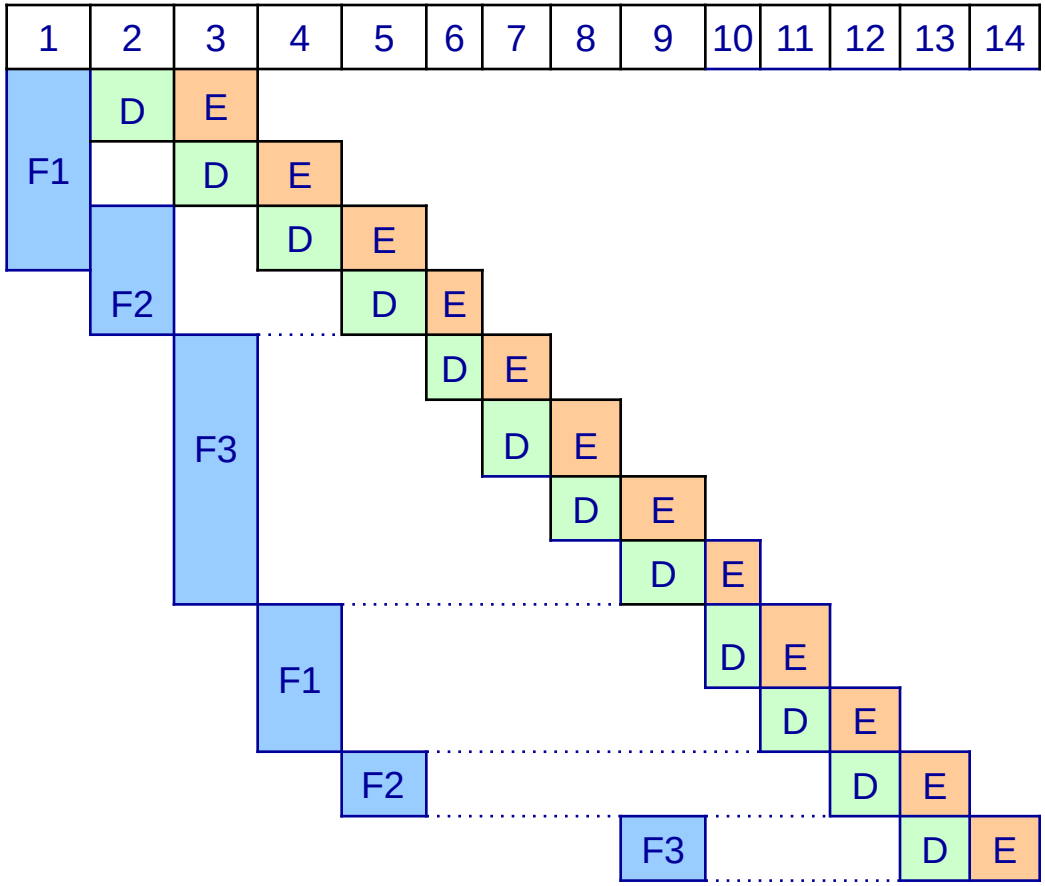
- The STM8 family uses a 3 stage pipeline in order to increase the speed of the flow of instructions to the processor.
  - Allows several operations to be undertaken simultaneously, rather than serially.



  - The PC points the instruction being decoded.

Optimal pipeline example

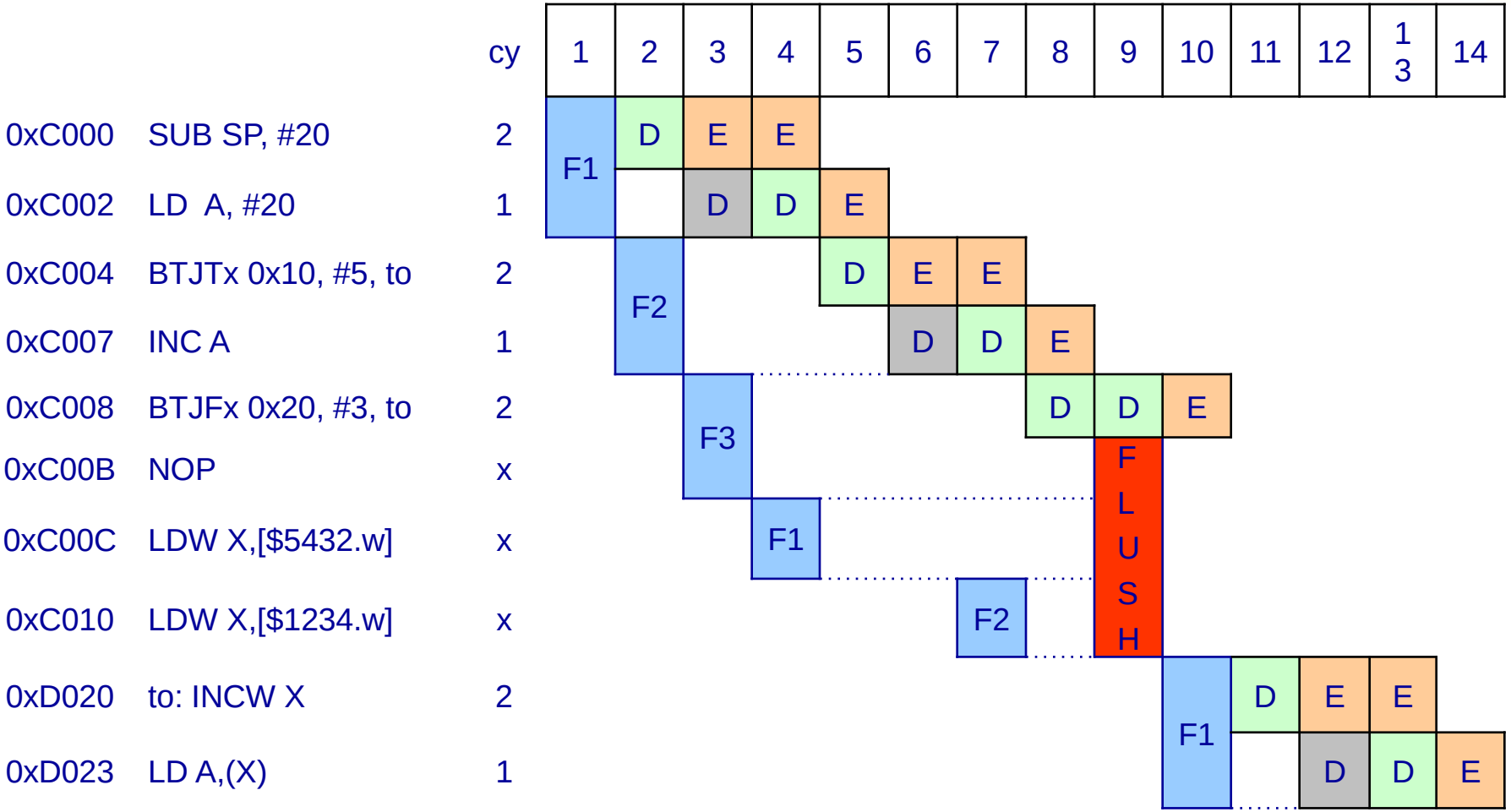
		cy	lg
0xC000	NEG A	1	1
0xC001	XOR A, $10	1	2
0xC003	LD X, #20	1	2
0xC005	SUB A,$1000	1	3
0xC008	INC X	1	1
0xC009	LD XL, A	1	1
0xC00A	SRL A	1	1
0xC00B	SWAP A	1	1
0xC00C	SLA $15	1	2
0xC00E	CP A,#$FE	1	2
0xC010	MOV $8000, #11	1	4
0xC014	MOV $8001, #22	1	4



F	Fetch	D	Decode	E	Execute

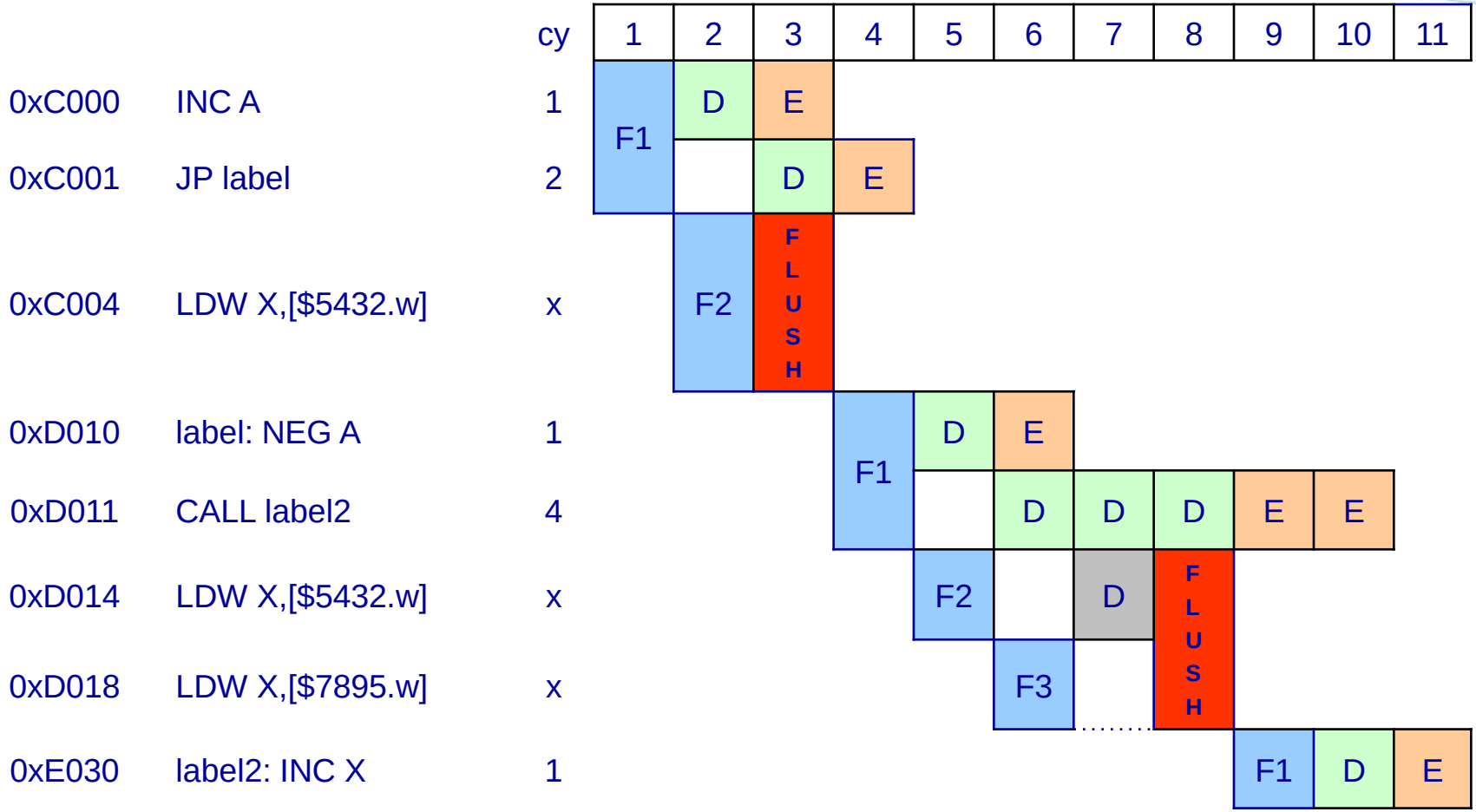
- Single cycle execution i.e. N instructions takes N clock cycles (CPI = 1)

Pipeline stalled example



F	Fetch	D	Decode	E	Execute	D	Decode Stall

Pipeline with Call/Jump



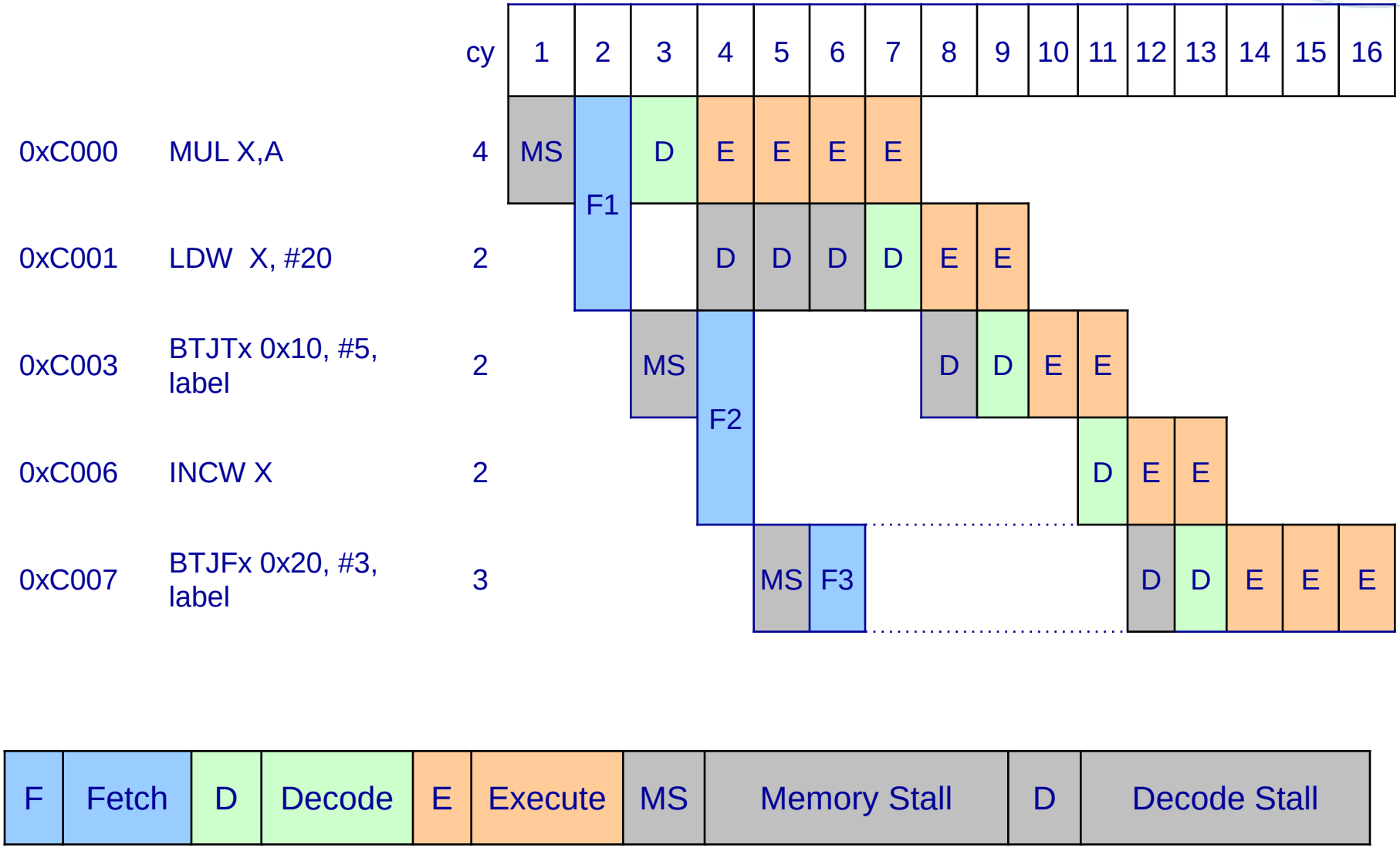
F	Fetch	D	Decode	E	Execute	D	Decode Stall

Optimal pipeline example with 1WS

		cy	1	2	3	4	5	6	7	8	9	10
0xC000	NEG A	1	MS	F1	D	E						
0xC001	DEC ($10, X)	1				D	E					
0xC004	LDW X, #20	2			MS	F2	D	E	E			
0xC007	LD (X), A	1						DS	D	E		
0xC008	INC A	1					MS	F3		D	E	
0xC009	NEG ($5A, Y)	1									D	E

F	Fetch	D	Decode	E	Execute	MS	Memory Stall

Pipeline stalled example with 1WS

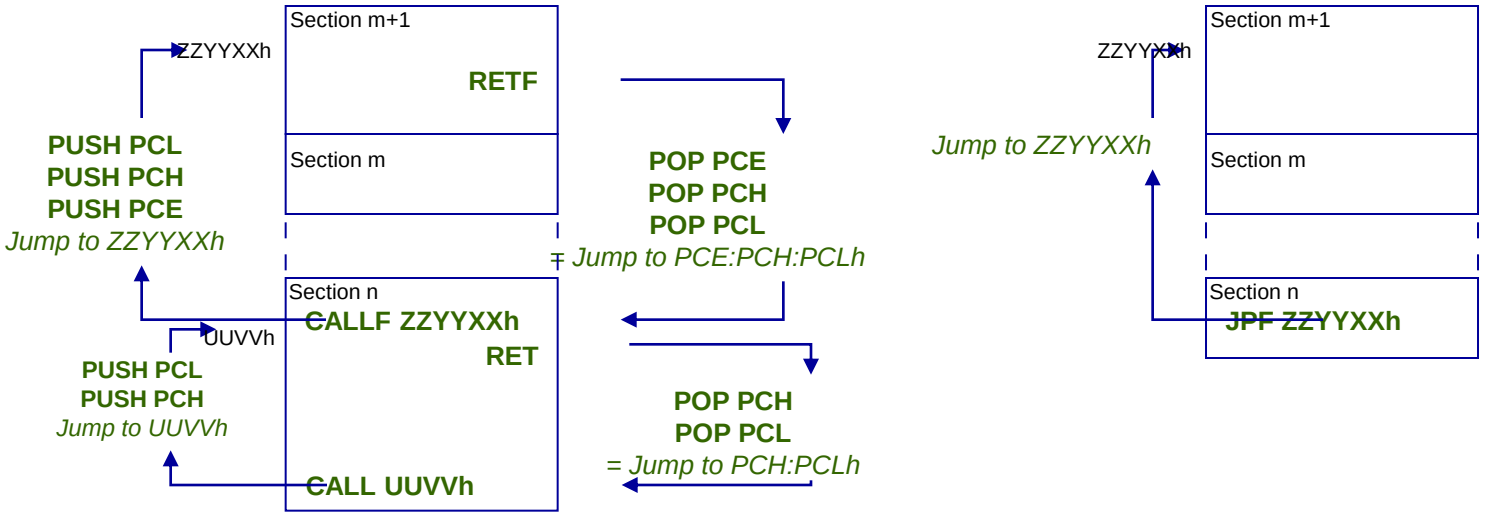


F	Fetch	D	Decode	E	Execute	MS	Memory Stall	D	Decode Stall

16MByte Memory Space Enhancements (1/

- **PROGRAM**: 16MByte linear memory space
  - Made up of 256 sections of 64-kbytes (example: section 0 is from 000000h to 00FFFFh)
  - 1 new CPU PCE register = Extended Program Counter

Program Counter is on 24-bit



New instructions to support this 24-bit PC

Instruction set

- **New addressing modes**
  - To take benefits of the 16-bit index registers
  - To access more efficiently the first 64k section
- **New instructions**
  - To handle 16-bit index registers
  - To improve compiler performance
  - To address the 16Mbyte memory space
  - To speed-up computation
    - Faster multiplication 8x8
    - 16-bit arithmetic instructions
  - To compute 16-bit operations
    - Division 16/8 and 16/16
  - To perform signed operation
    - V flag in CC

Instruction set evolution - Brand new instructions

- **MOV**
  - To allow fast (1-cycle) copy from a memory location to another without affecting the accumulator
  - Supports immediate and direct addressing modes on short and long addresses
- **WFE**
  - To allow synchronization with other computing resources
  - CPU is stopped but internal peripherals still running
  - Execution will continue when an external event will occur
  - Internal interrupts are served according to I[0:1]
  - Available on STM8L devices

Performance

- **Most instructions are executed in a single cycle**
  - Vs 3 to 4 cycles/instructions for ST7
- **Improved code efficiency (~30% smaller vs ST7)**
- **Leading edge 8-bit controller**
  - 0.29 DMIPS – similar to some well known 16-bit CPU performance
  - Twice as fast as 8-bit most used CPU (following standard industry benchmark)

STM8 vs ST7

Features	ST7	STM8
Addr Range	64KB Linear	**16MB Linear**
Architecture	Von Neumann CISC	**Harvard** **CISC**
Clocks per Instr. (CPI)	3 to 12	**3 Stage Pipe Line** **Avg 1.6 CPI**
ALU	8-bit	**8-bit &** **16-bit for address calculation**
Stack	8-bit SP	**16-bit SP with addr modes & stack/param allocation**
Other	8x8 Mul Bit handling on first page	**16-bit index pointers** **Long relative branch** **Fast 8x8 Mul;** **16/8 & 16/16 Division;** **Bit Handling on first section;** **Adv Debug Support**
Low Power	None	**Reduced data/fetch transfers; High instruction efficiency**

QUIZ

- What is new in core architecture ?
- What is the length of the index registers ?
- How many CPU cycles are needed for most of operations ?

New debug capabilities

- **SWIM** : **S**ingle **W**ire **I**nterface **M**odule
  - SWIM is both a protocol and a a communication cell with bus access capability
  - Faster protocol, running at HSI frequency
  - Cell can read on the fly without stalling the CPU
    - No more monitor using CPU resources
  - New shadow core registers
    - could be readed by SWIM on the fly without core stall
  - A pin is dedicated to SWIM communication
    - Can also be used as GPIO
    - Configuration in the CFG Global Configuration Register (CFG_GCR)

SWIM vs ICC

Functions	ICC	SWIM
Connections	VDD, VSS, Reset, IccData, IccClk, (VPP), (ext clock)	**VDD, VSS, Reset, SwimDbg**
Baud rate	20 kbytes at 8MHz	**144 kbytes at 16MHz**
Read/Write on the fly	intrusive	**RAM, Peripherals & (shadow) Core registers non intrusive**
Software monitor/TRAP interrupt reserved	Always	**Not needed**
Software breakpoints	TRAP	**SWBRK**
Hot plug (debug without reset)	Not possible	**Yes**

Non-intrusive SWIM access

Non-intrusive

- SWIM doesn't use any CPU resource. No restrictions for addresses and memory space.
  - No monitor code
  - No interrupt remapping

Real-time code execution

- SWIM steals dead cycles to read RAM and registers.
- Write accesses need to stop CPU execution.

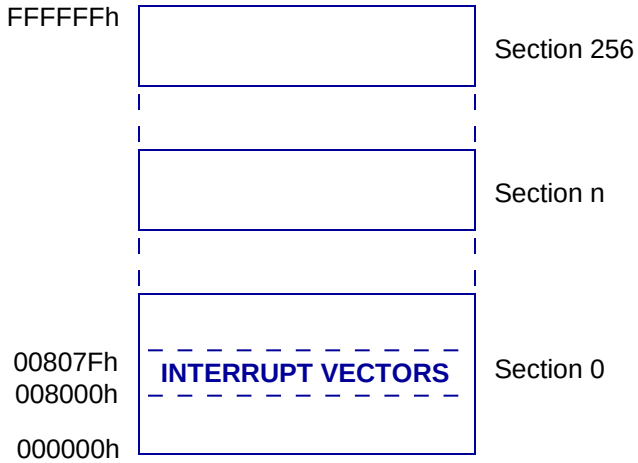
Interrupt management (1/5)

- **Up to 32 interrupt vectors**
  - At least one interrupt by peripheral
- **Nested or concurrent modes**
  - Software priorities programmable by ISPR registers
    - 3 levels + disable interrupts
- **A Top Level Interrupt (TLI)**
  - Managed by PD7
  - 2 sensitivities : falling edge or rising edge
  - Enabled by software
  - TLI can only be interrupted by TRAP or RESET
- **Set of external interrupts (5-12)**
  - Programmable sensitivity
- **Boot mode support**
  - For memory update (by UART, CAN, LIN)

Interrupt Management (2/5)

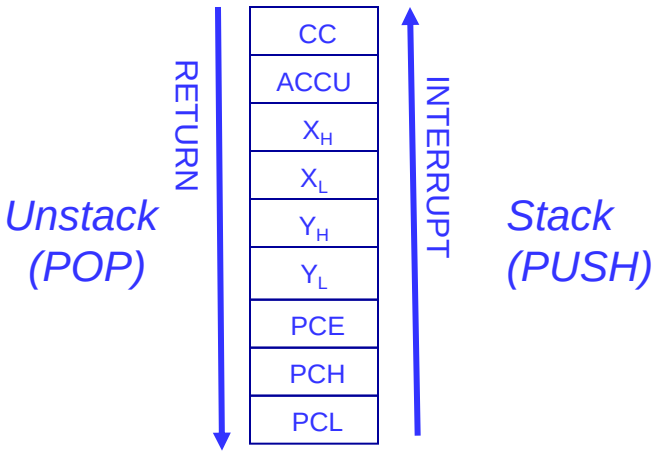
- **Interrupt vector table**
  - 32 extended vectors
  - Address >> 08000h-0807Fh on STM8 family
  - 1+3-byte interrupt vector = interrupt routine anywhere in the memory space

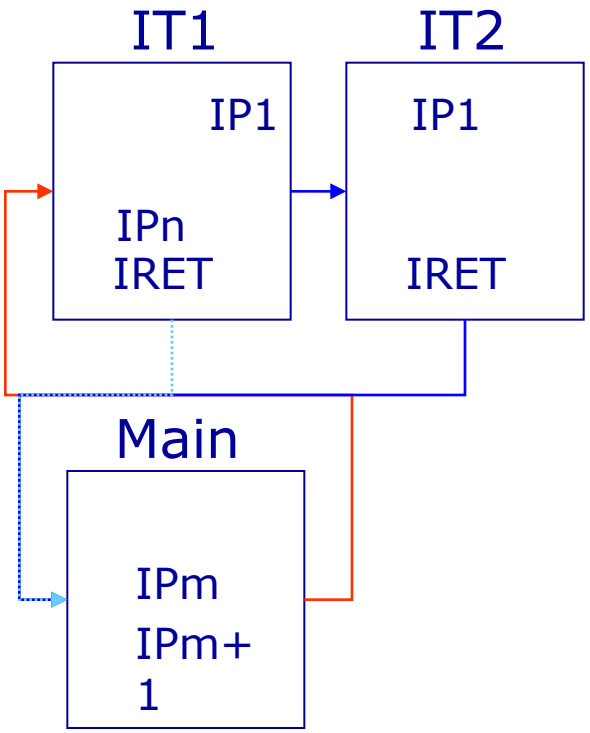
    Note: each vector table entry has 4-bytes – 1st byte contains the dedicated instruction opcode (**INT** - 82h)
  - Breakpoints not supported in the vector table



Interrupt Management (3/5)

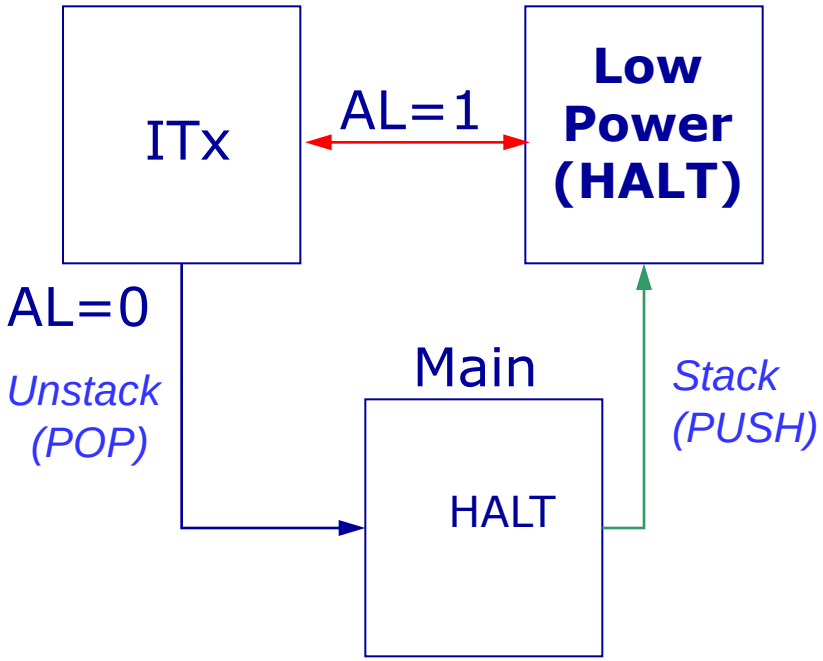
- **Interrupt and stack management**
  - full context save (A,X,Y,CC, PC)
  - 4 nested interrupt levels (with TLI and TRAP)
  - Tail chaining





Interrupt Management (4/5)

- **Activation level management**
  - **Used for low power modes**
    - Controlled by CFG_GCR – AL bit
    - Automatic return to HALT once ISR is finished
    - Configurable return to MAIN once ISR is finished
    - To maximize time ratio HALT mode / RUN mode



Interrupt Management (5/5)

- **Interrupt latency**
  - 9 cycles needed to save the context
  - Instruction in Exectue stage is always completed
    - Except for divisions (DIV and DIVW) which can be interrupted.
  - Some instructions shares Decode/Execution stage
    - Those cannot be interrupted even in decode
    - Typically instructions (re)storing context or accessing 16bit X/Y
  - Max latency is 15 cycles in case of CALLF indirect execution ($8T_{cpu}$) (context saving start on the last but one execution cycle)

- **Interrupt and fetch**
  - The current fetch and decode pipeline contents are lost after return from interrupt.

Quiz

- Where are located the interrupt vectors and how many are they ?
- What is the most prior external interrupt and what are the differences versus standard external interrupts ?
- What is stacked when an interrupt is served ?

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